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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JIMMIE EARL DEWITT JR., FRANK ELIOT LEVINE, ENIO MANUEL PINEDA, CHRISTOPHER MICHAEL RICHARDSON, and ROBERT JOHN URQUHART

Appeal 2009-003645
Application 10/675,778
Technology Center 2100

Decided: August 20, 2009

Before HOWARD B. BLANKENSHIP, CAROLYN D. THOMAS, and DEBRA K. STEPHENS, *Administrative Patent Judges*.

BLANKENSHIP, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

This is an appeal under 35 U.S.C. § 134(a) from the Examiner's final rejection of claims 1-25, which are all of the claims pending in this application. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

Invention

Appellants' invention relates to a method, apparatus, and computer instructions in a data processing system for processing instructions. An instruction is received at a processor in the data processing system. If an indicator is associated with the instruction in which the indicator identifies a threshold value, execution of the instruction is counted if a time for executing the instruction exceeds the threshold value. Responsive to a request to access data, a determination is made as to whether the indicator is associated with the data. The indicator identifies a threshold value. Access to the data is counted if the indicator is associated with the data and if a time needed to access the data exceeds the threshold value. (Abstract).

Representative Claims

1. A method in a data processing system for processing instructions, the method comprising:

responsive to receiving an instruction at a processor in the data processing system, determining whether an indicator is associated with the instruction, wherein a threshold value is located in the indicator; and

counting executions of the instruction if the indicator is associated with the instruction and if a time for executing the instruction exceeds the threshold value.

3. The method of claim 1, wherein the threshold value is a three bit value located in the indicator.

Prior Art

Davidson	6,446,029 B1	Sep. 3, 2002

Examiner's Rejections

Claims 1, 2, and 4-25 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Davidson.

Claim 3 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Davidson.

Claim Groupings

Based on Appellants' arguments in the Appeal Brief, we will decide the appeal on the basis of claims 1 and 3. *See* 37 C.F.R. § 41.37(c)(1)(vii).

ISSUES

(1) Have Appellants shown the Examiner erred in finding that Davidson discloses the limitations of claim 1?

(2) Have Appellants shown the Examiner erred in finding that a threshold value having three bits was a design step well within the grasp of a person of ordinary skill in the art at the time of invention?

FINDINGS OF FACT

1. Davidson discloses a method and system for monitoring the performance of an instruction pipeline. The occurrence of a specified event is monitored during the execution of an instruction in the execution pipeline of a processor. A particular instruction may be specified to execute within a

threshold time for each stage of the instruction pipeline. The specified event may be the completion of a single tagged instruction beyond the specified threshold interval for a stage of the instruction pipeline. The performance monitor may contain a number of counters for counting multiple occurrences of specified events during the execution of multiple instructions, in which case the specified events may be the completion of tagged instructions beyond a threshold interval for any stage of the multiple stages of the execution pipeline. As the instruction moves through the processor, the performance monitor collects the events and provides the events for optimization analysis. Abstract.

2. Fetch unit 501 (Fig. 5A) fetches instructions from memory. As an instruction is fetched, a single instruction may be selected and marked (or tagged). If only a single marked instruction proceeds through the pipeline, then the instruction is marked with a single bit. If multiple instructions are marked, then a tag consisting of multiple bits identifies marked instructions. Instructions may be marked based on a variety of selection mechanisms, each of which may be under the control of the performance monitor. Col 7, l. 51 to col. 8, l. 17.

3. Thresholder 520 (Fig. 5B) monitors the stage completion signals and compares the time intervals of each pipeline instruction stage with threshold values stored in threshold registers 521-525. If an instruction pipeline stage requires more time to complete than indicated by its corresponding threshold value, then thresholder 520 asserts a threshold event signal 526 that is collected by an event counter or multiple event counters 530 in the performance monitor. The performance monitor may merely

count such events for presentation to performance monitoring software. Col. 8, l. 59 to col. 9, l. 1.

4. The threshold values (605; Fig. 6A) may be temporal interval values with one value for each stage of the instruction pipeline. If specified, the instruction in the table entry is expected to execute within the specified temporal interval for each stage of the instruction pipeline. If the pipeline stage requires a greater amount of time to execute than the specified amount of time, an event may be triggered and collected by the performance monitor. Col. 9, ll. 25-33.

PRINCIPLES OF LAW

Claim Interpretation

During examination, claims are to be given their broadest reasonable interpretation consistent with the specification, and the language should be read in light of the specification as it would be interpreted by one of ordinary skill in the art. *In re Amer. Acad. of Sci. Tech Ctr.*, 367 F.3d 1359, 1364 (Fed. Cir. 2004) (citations omitted). The Office must apply the broadest reasonable meaning to the claim language, taking into account any definitions presented in the specification. *Id.* (citing *In re Bass*, 314 F.3d 575, 577 (Fed. Cir. 2002)).

Anticipation

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. Inc. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987).

Obviousness

The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, and (3) the level of skill in the art. *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966). "The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 416 (2007).

ANALYSIS

Claim 1

Appellants contend that Davidson does not disclose "counting executions of the instruction if the indicator is associated with the instruction and if a time for executing the instruction exceeds the threshold value" as recited in claim 1 (App. Br. 12). Appellants submit (App. Br. 6) that this claim recitation is described in the Specification at page 35, lines 4-10 , which states that a "determination is made as to whether the threshold has been exceeded for this instruction (step 1306) [Fig. 13]. If the threshold has been exceeded . . . a counter may be incremented."

The Examiner finds that Davidson discloses if an instruction pipeline stage requires more time to complete than indicated by its corresponding threshold value, then the thresholder asserts a threshold event signal that is collected by an event counter (Ans. 14).

We are not persuaded that the claimed "counting executions of the instruction if the indicator is associated with the instruction and if a time for

executing the instruction exceeds the threshold value," when read in light of Appellants' Specification, distinguishes over using an event counter to count the execution of the instruction having an execution time exceeding the threshold time as disclosed by Davidson.

Appellants also contend that the threshold values of Davidson are not located in an indicator associated with an instruction (App. Br. 13-14).

The Examiner finds that Davidson discloses an instruction tag for marking the instruction and threshold value registers that collectively comprise the claimed indicator (Ans. 3, 12-13). In response, Appellants contend that "marking of the instruction has nothing to do with a threshold value" (Reply Br. 3), and the

> threshold values are associated with the instruction pipeline stages and not with the instruction. Any marked instruction that flows through the pipeline stages will be monitored based on the same threshold values specified in the threshold registers. . . . Davidson, in fact, teaches away from the present invention by teaching that the threshold values are located in threshold registers that are associated with pipeline stages and that are separate from any indicator associated with an instruction.

Id.

When an instruction is marked by a tag, the thresholder monitors the stage completion signal of the marked instruction and compares the time intervals of each pipeline instruction stage with threshold values stored in threshold registers (FF 1, 3). Therefore, the threshold registers are "associated" with the marked instruction within the meaning of claim 1. The threshold registers are "indicators" because the threshold registers store threshold values that "indicate" an execution time for a marked instruction at a given stage in the pipeline (FF 3, 4). Therefore, each threshold register is

an indicator, associated with a marked instruction, having a threshold value for the marked instruction located in the indicator within the meaning of claim 1. Appellants have failed to provide evidence or persuasive arguments to rebut the Examiner's finding that the instruction tag and threshold value registers meet the indicator limitation of claim 1.

Appellants contend that Davidson does not disclose "determining whether an indicator is associated with the instruction" as recited in claim 1, because Davidson does not determine whether threshold registers are associated with instructions (App. Br. 14).

We disagree with Appellants' assessment of the Davidson reference. Davidson determines whether a threshold register is associated with an instruction by using a tag to identify an instruction as a marked instruction (FF 2). The threshold registers of Davidson are associated with marked instructions (FF 3).

Appellants also contend that Davidson does not perform the determining step "responsive to receiving the instruction at a processor in the data processing system" (Reply Br. 4). However, Davidson discloses marking the instruction as the instruction is fetched by a processor from memory (FF 2). The claimed "receiving an instruction at a processor" fails to distinguish over fetching the instruction from memory as disclosed by Davidson. Therefore, Davidson discloses "responsive to receiving an instruction at a processor in the data processing system, determining whether an indicator is associated with an instruction" as recited in claim 1.

Claim 3

Appellants contend that Davidson does not disclose or suggest that the threshold value is a three bit value located in the indicator (App. Br. 15). The Examiner finds that using three bits to represent a threshold value provides a benefit of allowing eight different values using a small amount of logic (Ans. 12). Appellants contend that this finding is based on impermissible hindsight (App. Br. 15-16).

Davidson does not explicitly state that the threshold value is a three bit value. However, a person of ordinary skill in the art is also a person of ordinary creativity, not an automaton. As noted by the Examiner, the artisan would recognize that three bits can represent eight different threshold values. The Examiner has provided a convincing rationale in support of why using three bits to represent a threshold value was a design step well within the grasp of a person of ordinary skill in the art at the time of invention. Appellants have provided no evidence to the contrary.

CONCLUSIONS OF LAW

(1) Appellants have not shown the Examiner erred in finding that Davidson discloses the limitations of claim 1.

(2) Appellants have not shown the Examiner erred in finding that a threshold value having three bits was a design step well within the grasp of a person of ordinary skill in the art at the time of invention.

DECISION

The Examiner's rejection of claims 1, 2, and 4-25 under 35 U.S.C. § 102(b) as being anticipated by Davidson is affirmed.

The Examiner's rejection of claim 3 under 35 U.S.C. § 103(a) as being unpatentable over Davidson is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED

msc

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